

An Isolated-Open Pattern to De-Embed Pad Parasitics

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Abstract—To meet radio frequency (RF) performance required in large market of wireless applications, CMOS transistors having a small unit gate width are preferred. To correctly estimate RF performance, parasitics of the on-wafer pads and interconnection metal lines should be de-embedded as in the advanced bipolar transistors. However, cutoff frequencies of small-size MOSFET's de-embedded by the conventional on-wafer dummy structures result in large overestimation. A new open pattern is proposed to solve the problem. The meaning and justification of the new de-embedding pattern are discussed.

Index Terms—Cutoff frequency, de-embedding, MOSFET.

I. INTRODUCTION

AS THE LARGE potential market for the low-power and wireless terminals is growing, the possibility of CMOS radio frequency (RF) IC has attracted much attention due to its low cost and compatibility to the analog process [1]. The RF performance of CMOS transistors has been enhanced by scaling down the gate length. In the conventional CMOS process with poly-Si gate, however, the noise figure is degraded and the speed is limited by high gate resistance. To reduce gate resistance, layout has been optimized by reducing gate width and using multifinger gate electrodes [2], [3]. As the gate width of CMOS transistors shrinks, the effect of on-wafer contact pads and interconnection metal lines on RF performance should be de-embedded specially for the MOSFET's in low-power applications. Several methods to de-embed on-wafer parasitics by dummy structures have already been proposed in advanced bipolar characterization [4]–[7].

In this letter, we show that direct application of the conventional method to small-size CMOS transistors causes large overestimation in cutoff frequencies. The errors are attributed to using the conventional open pattern. Therefore, a new isolated-open pattern is proposed to solve the problem.

II. SEQUENCE OF DE-EMBEDDING

A two-step method using two dummy patterns (open and short) is used for de-embedding [7]. Among them a new isolated-open pattern is used instead of the conventional dangling-open pattern (see Fig. 1). The isolated-open pattern is simply one of the dangling-open patterns when the separation between dangling edges of interconnection metal lines is far enough to neglect coupling capacitances C_{ij} 's in Fig. 2.

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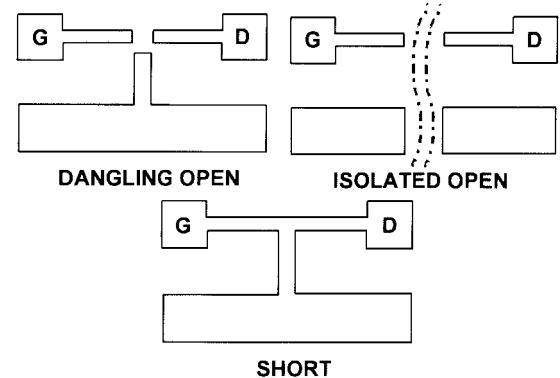


Fig. 1. Layout of the conventional dangling-open and short patterns, and the proposed isolated-open pattern.

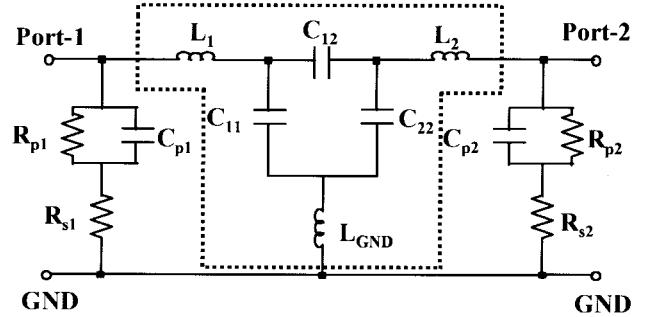


Fig. 2. The lumped-element equivalent circuit of the dangling-open pattern. When the elements in dotted box are absent, this results in the equivalent circuit of the isolated-open pattern. When the coupling capacitances in dotted box are shorted, this results in the equivalent circuit of the short pattern.

Although all the de-embedding procedure has been performed by algebraic calculation using measured s -parameters of short and open patterns, numerical extraction of parasitics of two dummy structures has been also performed to get a quantitative view. The procedure of numerical extraction is given below. The equivalent circuit of the isolated-open pattern is shown in Fig. 2 if the elements in the dotted box are absent. When $\omega^2 C_{pi}^2 (R_{pi} // R_{si})^2 \ll 1$ and $R_{si} \ll R_{pi}$, the y -parameter expression of the isolated-open pattern can be simplified to

$$y_{ij} \approx \begin{cases} (1/R_{pi}(1+\omega^2 C_{pi}^2 R_{pi} R_{si}) + j\omega C_{pi}), & \text{for } i = j = 1, 2 \\ 0, & \text{for } i \neq j. \end{cases} \quad (1)$$

Values of dangling open parasitics can be easily obtained by fitting the frequency versus open y -parameters to (1). The equivalent circuit of the short pattern is shown in Fig. 2 if the coupling capacitances C_{ij} 's are shorted. Series inductances

TABLE I

VALUES OF THE LUMPED ELEMENTS OF OPEN AND SHORT PATTERNS
OBTAINED FROM NUMERICAL EXTRACTION ($i = 1$ AND 2)

C_{pi}	C_{ii}	C_{12}	R_{pi}	R_{si}	L_1, L_2	L_{GND}
5.2 fF	4.6 fF	4.8 fF	54 k Ω	124 Ω	76 pH	71 pH

of interconnection metal lines can be extracted by fitting the frequency dependence of z -parameters of the short pattern after de-embedding the isolated-open elements [8]. Then, the coupling capacitances C_{ij} 's of dangling-open pattern can be obtained by optimizing the measured s -parameters of dangling-open pattern, while keeping the isolated-open and short parasitics unchanged.

III. MEASUREMENTS AND RESULTS

The test devices are multifinger n -MOSFET's of 0.8- μm analog CMOS technology having optimized unit gate width of 10 μm [3]. The substrate is high-resistivity silicon (2–5 k $\Omega \cdot \text{cm}$) and its benefit has been demonstrated elsewhere [9]. All the parasitics obtained from numerical extraction are summarized in Table I.

The effect of number of gate fingers on the cutoff frequency is shown in Fig. 3. The cutoff frequency f_t of the conventional two-step de-embedding method (using dangling-open and short patterns) abruptly increases as the number of gate fingers decreases, especially for the gate finger of one and two, while weak and smooth dependence is observed in case of the new method (using isolated-open and short patterns). There is no reason for the drastic change in cutoff frequency for small number of gate fingers. The dependence of cutoff frequency on the drain current for an n -MOSFET having two unit gate fingers is shown in Fig. 4. The difference in f_t 's for two de-embedding methods are more than 50%. The third data shows f_t calculated by the formula $f_t = g_m/2\pi(C_{gs} + C_{gd})$. The capacitances and transconductances are estimated from BSIM3v2 parameters extracted by using UTMOST. The calculated f_t supports the validity of our de-embedding method. Using the extracted parasitics in Table I, the effective capacitance value seen by the port-1 or port-2 for the dangling-open pattern is about 12.9 fF if the effect of parasitic resistances and inductances is ignored. The sum of gate-source and gate-drain capacitance ($C_{gs} + C_{gd}$) is about 30 fF for an n -MOSFET having two unit-gate fingers. Roughly speaking, $(C_{gs} + C_{gd})$ is reduced by 12.9 fF for the conventional de-embedding method. Therefore, cutoff frequency is expected to be overestimated by more than 50% when de-embedding is done by the dangling-open parameters. In addition, there are two more reasons for the justification of using the isolated-open pattern. First, the coupling capacitances C_{ij} 's are not identical to those when the active device is inserted because coupling field profile is changed by ohmic regions of higher doping concentration and metal electrodes after device insertion. The other is that even if the existence of the coupling capacitances is accepted, the major portion of the capacitive coupling comes from the RF potential differences between gate, source, and drain electrodes, which are parts of the actual device. Therefore, the

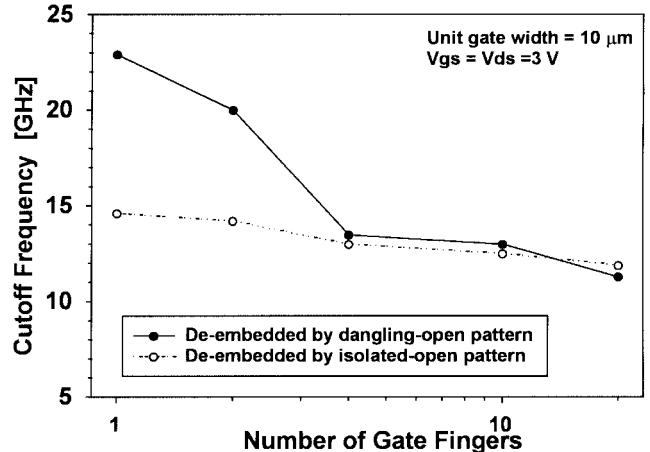


Fig. 3. Cutoff frequency of multifinger n -MOSFET's having 10- μm unit gate width. The bias point is fixed to $V_{ds} = V_{gs} = 3$ V.

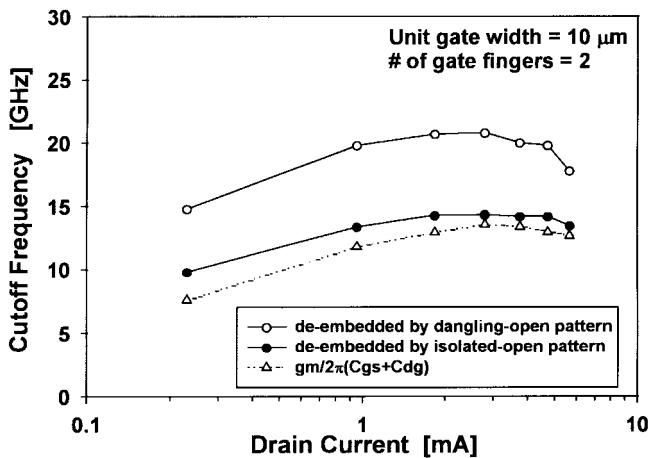


Fig. 4. The dependence of cutoff frequency on drain current for an n -MOSFET having two unit-gate fingers and 10- μm unit-gate width. The drain-source voltage V_{ds} is 3 V.

coupling capacitances should not be de-embedded if the real performance of the active devices is to be estimated.

IV. CONCLUSIONS

Since the conventional on-wafer de-embedding open pattern results in large errors in estimating cutoff frequencies for the small-size Si MOSFET's, a new open pattern, called isolated open, is proposed to de-embed on-wafer pad parasitics. By de-embedding open parasitics using this pattern, the errors in estimating cutoff frequency have been corrected. This pattern is expected to be used to de-embed on-wafer parasitics for small-size active devices.

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REFERENCES

- [1] N. Suematsu, "On-chip matching Si-MMIC for mobile communication terminal application," in *1997 IEEE RFIC Dig. Tech. Papers*, 1997, pp. 9–12.

- [2] S. P. Voinigescu *et al.*, "An assessment of the state-of-the-art $0.5 \mu\text{m}$ bulk CMOS technology for RF applications," in *Proc. IEDM-95*, 1995, pp. 721-724.
- [3] C. S. Kim *et al.*, "CMOS layout and bias optimization for RF IC design applications," in *IEEE MTT-S Dig. Tech. Papers*, 1997, pp. 945-948.
- [4] A. Fraser *et al.*, "GHz on-silicon wafer probing calibration methods," in *Proc. IEEE 1988 Bipolar Circuits and Technology Meeting*, Sept. 1988, pp. 91-94.
- [5] P. J. van Wijnen *et al.*, "A new straightforward calibration and correction procedure for on-wafer high-frequency S-parameter measurements (45 MHz-18 GHz)," in *Proc. IEEE 1987 Bipolar Circuits and Technology Meeting*, Sept. 1987, pp. 70-73.
- [6] H. Cho *et al.*, "A three-step method for the de-embedding of high-frequency *s*-parameter measurements," *IEEE Trans. Electron Devices*, vol. 38, pp. 1371-1375, June 1991.
- [7] M. C. A. M. Koolen *et al.*, "An improved de-embedding technique for on-wafer high-frequency characterization," in *Proc. IEEE 1991 Bipolar Circuits and Technology Meeting*, 1991, pp. 188-191.
- [8] G. D. Dambrine *et al.*, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1151-1159, July 1988.
- [9] M. Park *et al.*, "High *Q* CMOS-compatible microwave inductors using double-metal interconnection silicon technology," *IEEE Microwave Guided Wave Lett.*, vol. 7, pp. 45-47, Feb. 1997.